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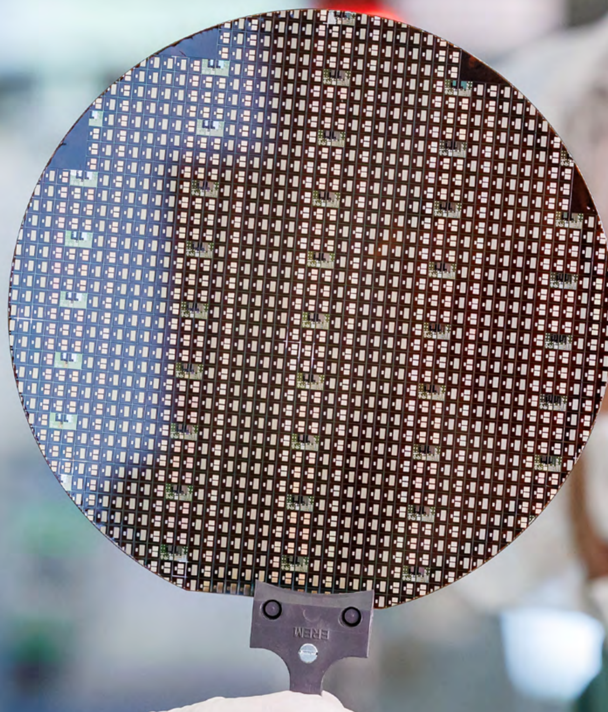
Fraunhofer Institute for Integrated Systems and Device Technology IISB



Processed 150 mm SiC Wafer

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SiC Devices

Custom-tailored Processes & Prototypes

One-stop Solution for the Development and Prototype Fabrication of SiC Devices

Fraunhofer IISB offers R&D services on SiC from materials development and prototype devices to module assembly and mechatronic systems.

Advantages & benefits

- Feasibility check and feedback regarding design
- Short development cycles due to full π-Fab access
- Electrical characterization, dicing, and inking service
- Small-volume production available for customer specific devices
- Less R&D costs and short time-to-market for your devices
- Reduced work effort due to all-in-one solution
- Competitive fabrication costs even at small volumes

Features

- In-house device simulation, fabrication, and characterization
- Hands-on experience on power semiconductor devices across full value chain
- Complete in-house technology from epitaxy, implantation, and trench patterning to device packaging and module assembly in a fully equipped 150 mm SiC pilot line
- Quality management and statistical process control

Prototype fabrication for power electron devices and detectors

Front-end processing

- Photolithography: mask aligner and stepper for resolutions down to 0.8 µm
- Wet chemistry for cleaning and etching
- Ion implantation up to 800 keV, with wafer heating (500 °C) up to 400 keV
- Advanced reactive ion etching of trenches in SiC
- Annealing (furnace and lamp heated) up to 1750 °C in various atmospheres
- Thermal oxidation in N2O for high channel mobilities
- LPCVD, PECVD, and ALD for dielectric and polysilicon deposition

Metallization and packaging

- Contact formation (Ohmic and Schottky) by RTP and laser annealing / wafer thinning
- Deposition and patterning of metallization layers for operation temperatures up to 500 °C
- Passivation by silicon based materials or polyimide
- Soldering and sintering processes as well as wire bonding for packaging

Electron devices and test patterns

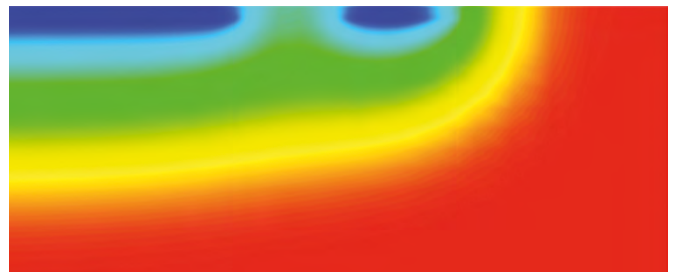
- Design and fabrication of test structures
- Manufacturing of power electronic and sensor devices

Characterization

- Electrical characterization of devices (I-V, C-V) up to 500 °C
- Static and dynamic characterization of high-voltage devices up to 100 A
- Parameter analysis of MOSFET devices
- Wafer prober for reliability assessment up to 10 kV

Simulation and modeling

- TCAD modeling of SiC devices
  - Models for channel mobility and avalanche prediction
  - Optimization of cell pitch and junction termination
- Extraction of SPICE models for circuit simulations
- Process simulation, e.g., for trench devices



Simulated distribution of electric field in the vicinity of JTE.
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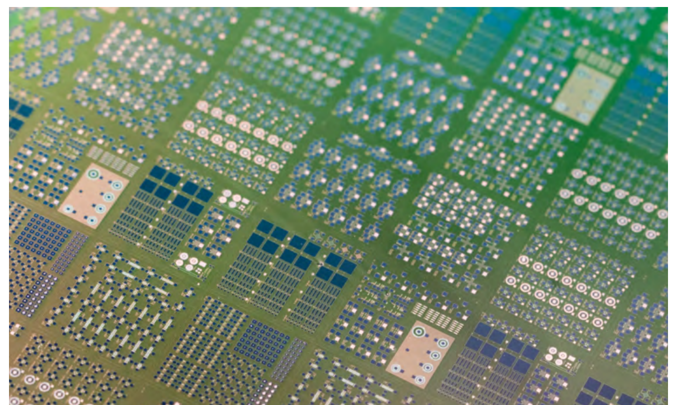

Top view of a 4H-SiC wafer with various types of electron devices: n- and p-channel MOSFETs, MOS-gated Hall bars, JFETs, PiN diodes, lateral IGBTs, test patterns.
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