International Conference on Silicon Carbid and Related Materials, September 29th – October 4th 2024, Raleigh, USA

On the Relationship of Processing Parameters and Epitaxial Defects to Extrinsic Failure in SiC Gate Oxide

H. Schlichting[1], T. Becker[1], L. Baier[1], M. Rommel[1], T. Erlbacher[2) 3)]

holger.schlichting@iisb.fraunhofer.de

1) Fraunhofer IISB, Schottkystr. 10, 91058 Erlangen, Germany
2) FAU Chair of Electron Devices, Cauerstr. 6, 91058 Erlangen, Germany
3) Nexperia Germany GmbH, Stresemannallee 101, 22529 Hamburg, Germany

Importance of gate oxide yield and reliability

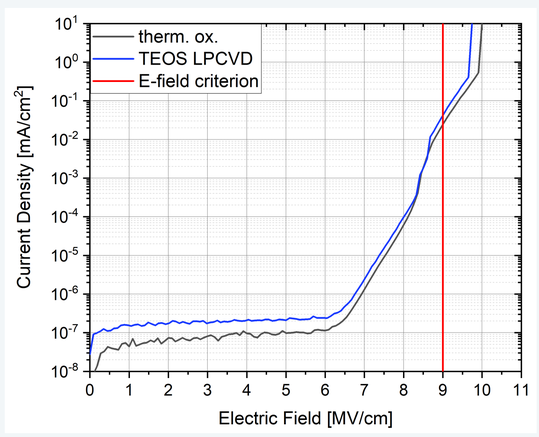
- 4H-SiC power devices are rapidly conquering the power semiconductor markets and are more and more implemented in commercial systems [1].
- The gate oxide is one of the most critical components in a 4H-SiC VDMOS transistor. Therefore, the focus of research has mostly been on the optimization of gate oxides by interface-engineering for improvement of mobility and threshold voltage [2].
- Regarding the reliability of gate oxide, the investigation of intrinsic gate oxide failure was prioritized [3]. The next step is to investigate the failure mechanisms of the SiO_2 on SiC in terms of electrical yield, namely initial gate oxide failure, and the extrinsic failures in the device lifetime. A correlation of yield and epitaxial defects was already shown in past investigations [4].

Overview of experiments

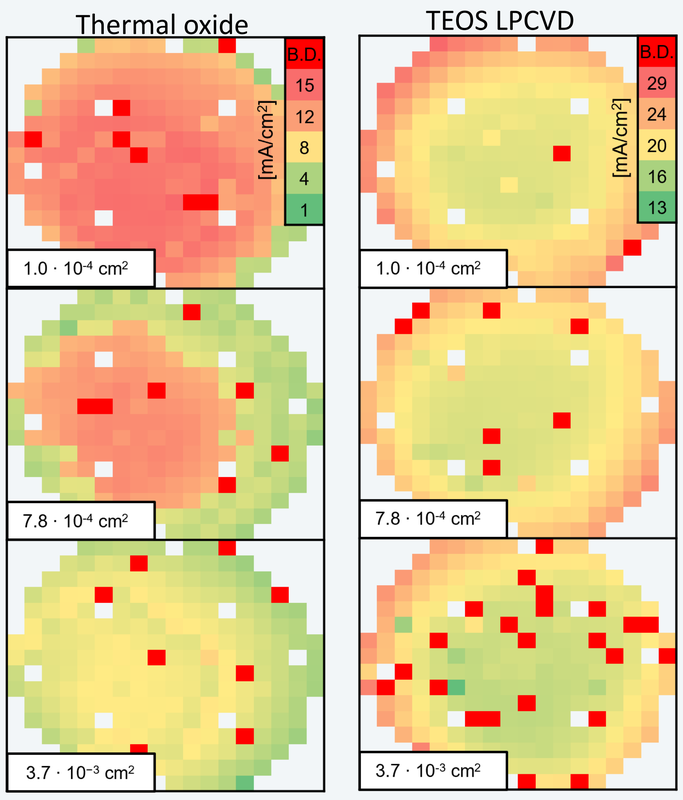
- Fabrication of MOS capacitors of different sizes on 4H-SiC epitaxial-wafers, with in-situ n-doped polysilicon as gate electrode.
- The methods of TZDB[a)] and TDDB[b)] with CCS[c)] are used as characterization techniques for evaluation of etb[d)] and ttb[e)].
- Two different oxides are investigated, one grown by dry thermal oxidation on the SiC epitaxial layer, one deposited by LPCVD[f)] with TEOS[g)] as a precursor.
- Epitaxial defect detection on samples before fabrication of MOS structures for correlation of field- and time-dependent failure.

Time-zero dielectric breakdown

- Voltage ramp is applied to MOS capacitors until dielectric breakdown is reached. Leakage current and premature breakdown are investigated at regimes of increased electric fields in the oxide.



Typical IV-Characteristic from TZDB-measurement for MOS capacitor samples with thermally grown and TEOS LPCVD oxide. Red Line marks field strength of 9 MV/cm for current density wafer maps below.

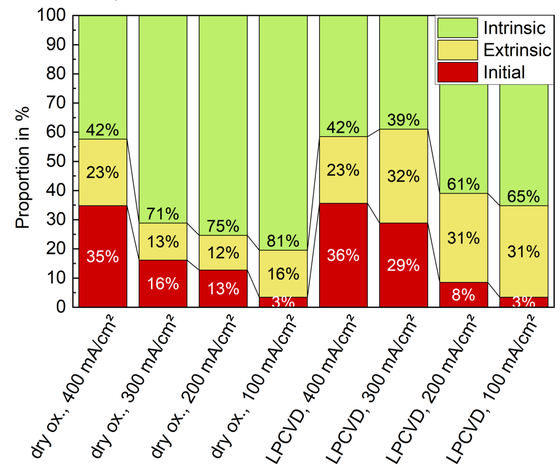


Current density distribution over both samples for different MOSCAP-sizes. While there is a trend for change of leakage current towards the edge, the devices with breakdown (B.D.) are randomly distributed.

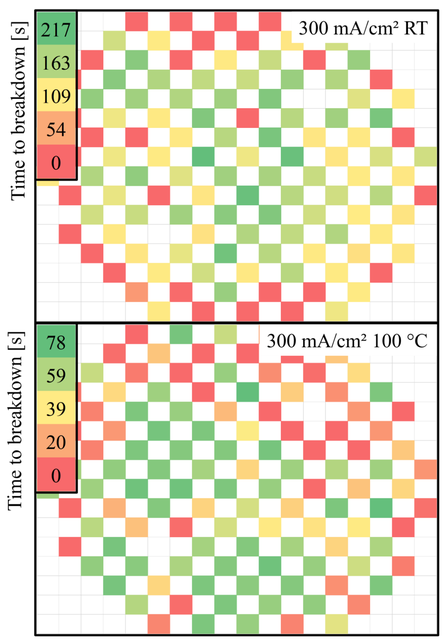
- While thermal oxide shows less defectivity in terms of B.D., the increase of failure for TEOS LPCVD sample is stronger with increase of MOS capacitor size.
- Leakage current distribution is inverted (center-edge).

Time-dependent dielectric breakdown – initial, extrinsic and intrinsic failure regimes and failure/defect-distributions

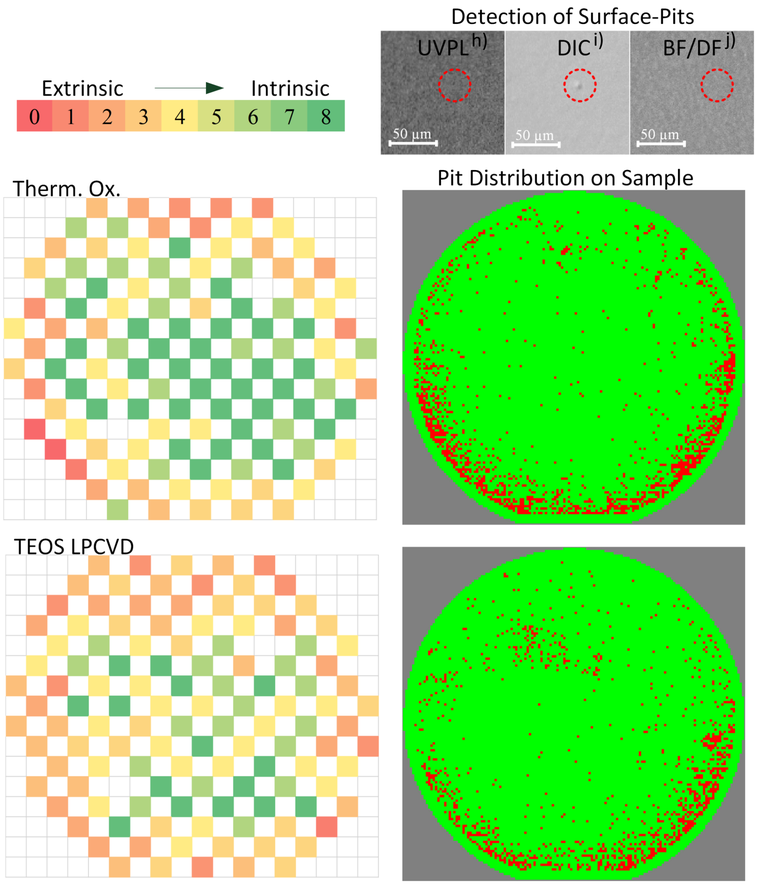
- In the ttb distribution (Weibull, not shown here), initial failure is defined as breakdown within the first two seconds of measurement, including current-ramp to stress-current. Narrow-distributed breakdowns at the end of the lifetime distribution are considered as intrinsic failure. Extrinsic failures are oxide breakdowns between initial and intrinsic parts of failure-distribution.



Ratio of initial failure, extrinsic failure, and intrinsic failure for the different CCS-values for both samples.



Time to breakdown distribution for measurement with CCS of 300 mA/cm² at room temperature (RT) and at 100 °C. Initial breakdown tending to be located at the edge, extrinsic breakdown is more randomly distributed. At higher temperature, average and maximum ttb is decreasing, ratio of extrinsic failure is increasing.



Mapping of the MOS capacitor positions with color coding represents the tendency of the respective position to extrinsic or intrinsic defect behavior over the measured current densities for both samples (left). Distribution of the surface-pits detected in the DIC channel for both samples (right). The wafer is divided into a virtual grid with an edge length of 1 mm. Appearance of surface-pits on epitaxial layer for different measurement channels is shown above the distribution maps.

- Defect activation by increasing current stress as well as increased temperature is indicated for both sample types.
- Tendency for external failure for TDDB can be correlated to surface pit distribution (only detectable in DIC-image).

Conclusion:
Experiments indicate that failure rate and probability is dependent on the applied electric field, temperature and current stress. Surface pits are suspected to be the cause of early (extrinsic) failure in device lifetime.

1 X. Yuan, IECON 2017, Beijing, pp. 893-900 (2017).
2 K. Tachiki et al., Appl. Phys. Express 14, 031001 (2021).
3 K. P. Cheung, J. Appl. Phys. 132, 144505 (2022).
4 H. Schlichting et al., Mater. Sci. Forum Vol. 1090, pp.127-133 (2023).

a) TZDB = time-zero dielectric breakdown
b) TDDB = time-dependent dielectric breakdown
c) CCS = constant current stress
d) etb = electric field to breakdown
e) ttb = time to breakdown
f) LPCVD = low pressure chemical vapor deposition
g) TEOS = Tetraethylorthosilicate
h) UVPL = ultraviolet photo luminescence
i) DIC = differential interference contrast
j) BF/DF = bright field/dark field imaging