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Gate Oxide Performance and Reliability on SmartSiC™ Wafers and the Influence of RTA processing on Gate Oxide Lifetime

Tom Becker[1], Mathias Rommel[1], Holger Schlichting[1], Leander Baier[1], Eric Guiot[2], Frédéric Allibert[2]

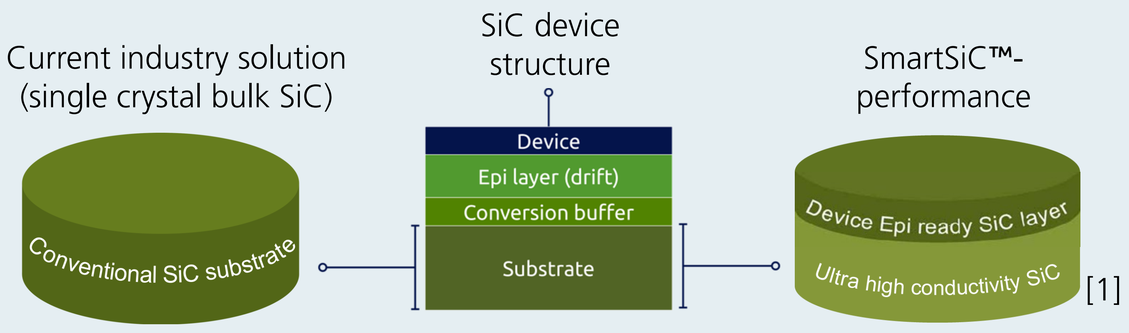
tom.becker@iisb.fraunhofer.de

[1] Fraunhofer IISB, Schottkystr. 10, 91058 Erlangen, Germany
[2] Soitec, Parc Technologique des Fontaines, 38190 Bernin, France

Motivation and Processing

- Comparison of standard 4H-SiC bulk substrates and Soitec's SmartSiC™ in terms of yield and reliability of MOS devices
- Investigation of the influence of RTA processing on the flat band voltage and oxide lifetime

SmartSiC™: optimum design for a unique value proposition



[1]

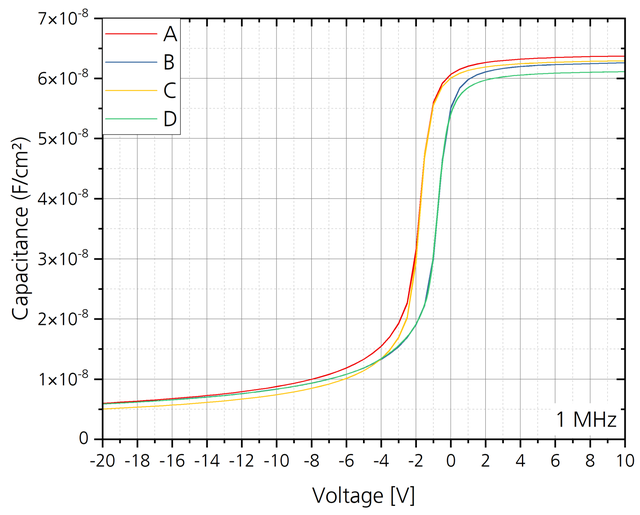
Wafer and process splits

#	Wafer Type	RTA
A	Standard bulk SiC + Epi	yes
B	Standard bulk SiC+ Epi	no
C	SmartSiC™ + Epi	yes
D	SmartSiC™ + Epi	no

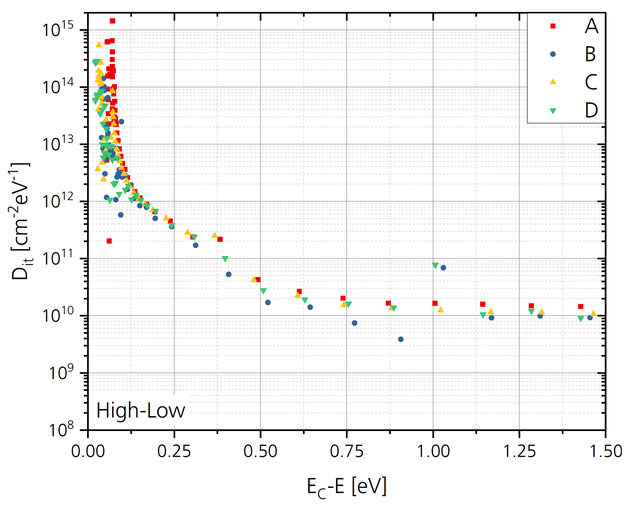
Dry Oxidation (1300 °C) → PolySi deposition (570 °C) → PECVD Field Oxide deposition (~250 °C) → Optional RTA (980 °C) → Metallization (~200 °C)

Electrical Characterization

CV measurements to determine V_{FB} and assess interface trap densities

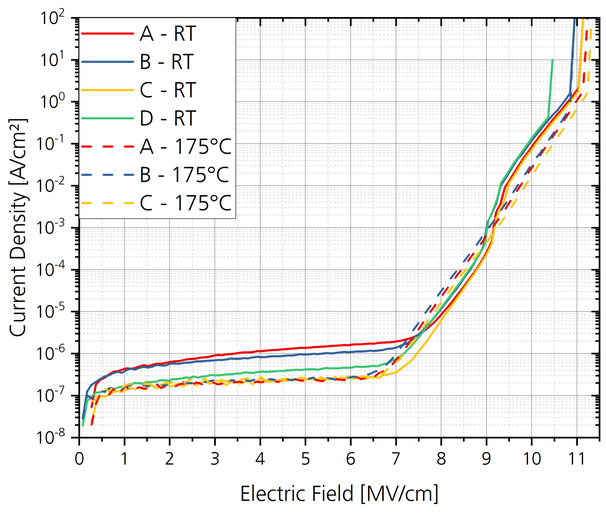


- No distinction between Bulk SiC and SmartSiC™
- > 1 V shift of V_{FB}, assumed partially due to incomplete dopant activation in the polysilicon gate electrode [2] in the absence of RTA

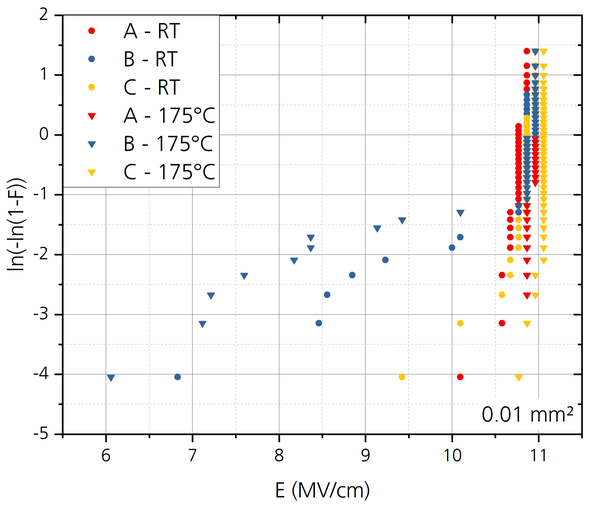


- D_{it} characteristics from High-Low and Terman (see paper) methods show no significant distinction between all samples

TZDB measurements to determine oxide quality and MOS capacitor yield

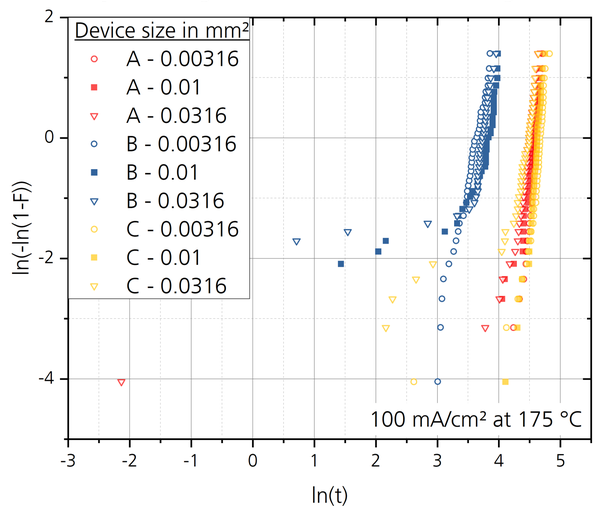


- Breakdown behavior of all samples overlap independent of measurement temperature, electric field calculated with consideration of different V_{FB} values

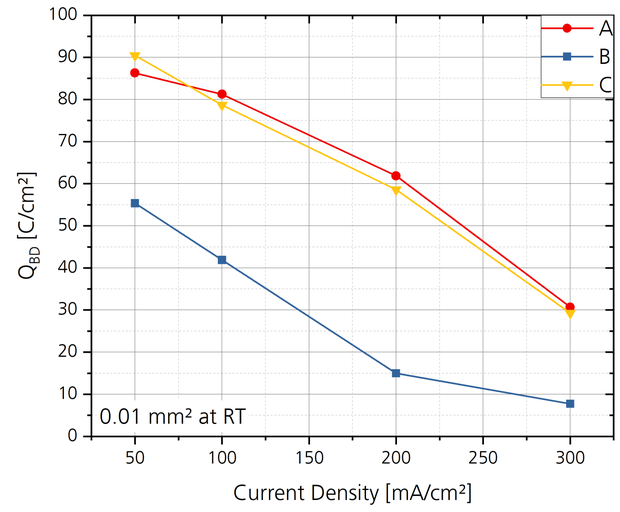


- Yield analysis for all sizes and temperatures display no notable differences between standard bulk substrates and SmartSiC™ material
- Non-RTA samples demonstrate more early failures

CCS-TDDB testing and Q_{BD} determination to quantify the oxide reliability



- Weibull plots of TDDB investigations at different temperatures and device sizes show a clear gap in oxide lifetime between RTA and non-RTA processed wafers



- Both CCS-TDDB and Q_{BD} extraction at a failure rate of 63 % show identical oxide reliability behavior for SmartSiC™ and standard bulk wafers

Conclusion

- After extensive analysis of MOS capacitors on both SmartSiC™ and standard bulk 4H-SiC wafers, no measurable differences were discovered.
- Skipping the RTA step induces a > 1 V shift in the V_{FB} and degrades the oxide reliability (over 30 % reduction in TDDB and Q_{BD}). The origin was suggested to be partially caused by incomplete activation of the phosphorous doped polysilicon gate electrode. Other possible contributions are still under investigation.

1 N. Daval et al., 6th IEEE Electron Devices Technology & Manufacturing Conference, pp. 85-87, 2022
2 S. Kallel, Materials Science in Semiconductor Processing, Volume 1, Issues 3–4, p. 299-302 (1998)

TRANSFORM
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