International
Conference on
DC Microgrids

Exploration of Use-Case-Dependent Modeling Approach for Distributed DC-Grids

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MOTIVATION AND APPLICATION

Designing DC grids is hard!

- **System design requires time, money and effort**
- **Simulations are essential for system design**
  - Cost efficient
  - Adjustable and scalable
- **Lack of verified models and ready-to-use tools for DC systems**
  - Models are developed for individual and specific applications
  - Simulation and analysis requires in-depth knowledge

⇒ **Model library with verified models for DC components**

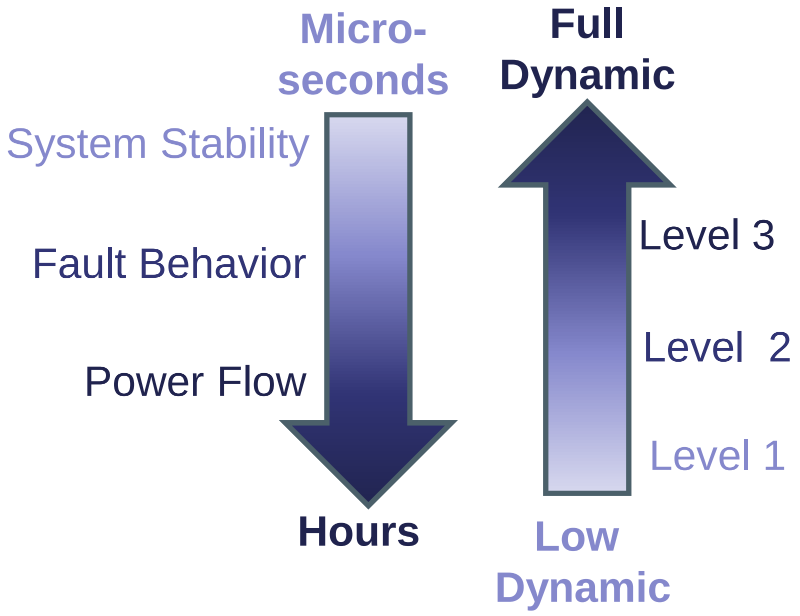
MOTIVATION AND APPLICATION

Use-Case-Dependent modeling approach for resource efficient simulation

- **Quality of results and computing resources depend on modeling approach**
  - Simulation of dynamic behavior requires high model complexity
  - Complex models increase computing resources

- **Introduction of *Use Cases* and *Model Levels***
  - Definition of three *Use Cases* for different evaluations
  - *Model Levels* are tailored to requirements of *Use Cases*

➡ **Verification of simulated system behavior**


Micro-seconds

System Stability

Fault Behavior

Power Flow

Hours

Full Dynamic

Level 3

Level 2

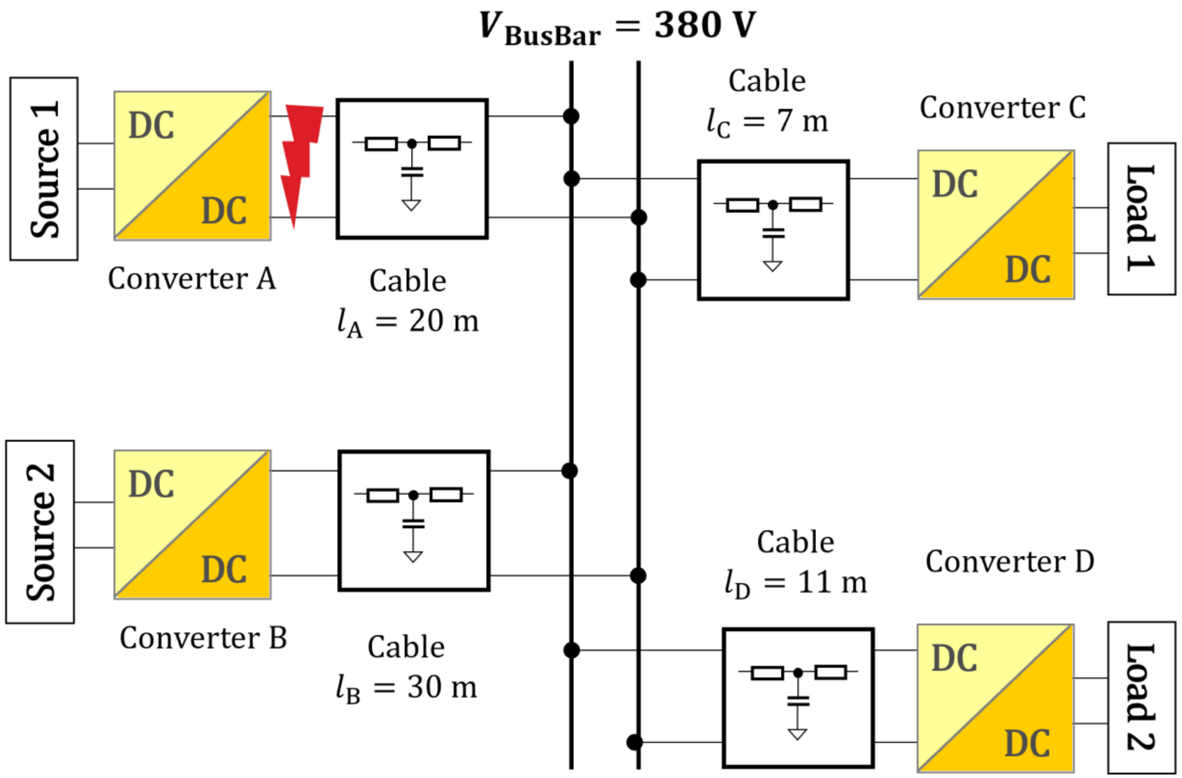
Level 1

Low Dynamic

MOTIVATION AND APPLICATION

Test grid for simulation verification

- Test grid with four DC-DC converters
- Cables with differing lengths to connect converters to bus bar
- Short circuit at outport of Converter A



$$C_{\mathrm{out,A}} = 33\ \mu\mathrm{F},\ C_{\mathrm{out,B}} = 226\ \mu\mathrm{F},\ C_{\mathrm{in,C}} = 33\ \mu\mathrm{F},\ C_{\mathrm{in,D}} = 153\ \mu\mathrm{F}$$

$$R_{\mathrm{Droop,A}} = 6\ \Omega,\ R_{\mathrm{Droop,B}} = 2\ \Omega,\ P_{\mathrm{set,C}} = 1\ \mathrm{kW},\ P_{\mathrm{set,D}} = 2\ \mathrm{kW}$$

$$L' = 1\mu\frac{\mathrm{H}}{\mathrm{m}},\quad R' = 0.75\ \mathrm{m}\frac{\Omega}{\mathrm{m}}$$

AGENDA

1. **Motivation and Application**
2. **Buck Converter Modeling**
   a) Level 3
   b) Level 2
   c) Level 1
3. **Line Models – All Levels**
4. **Simulation vs. Measurements**
5. **Conclusions and Further Works**

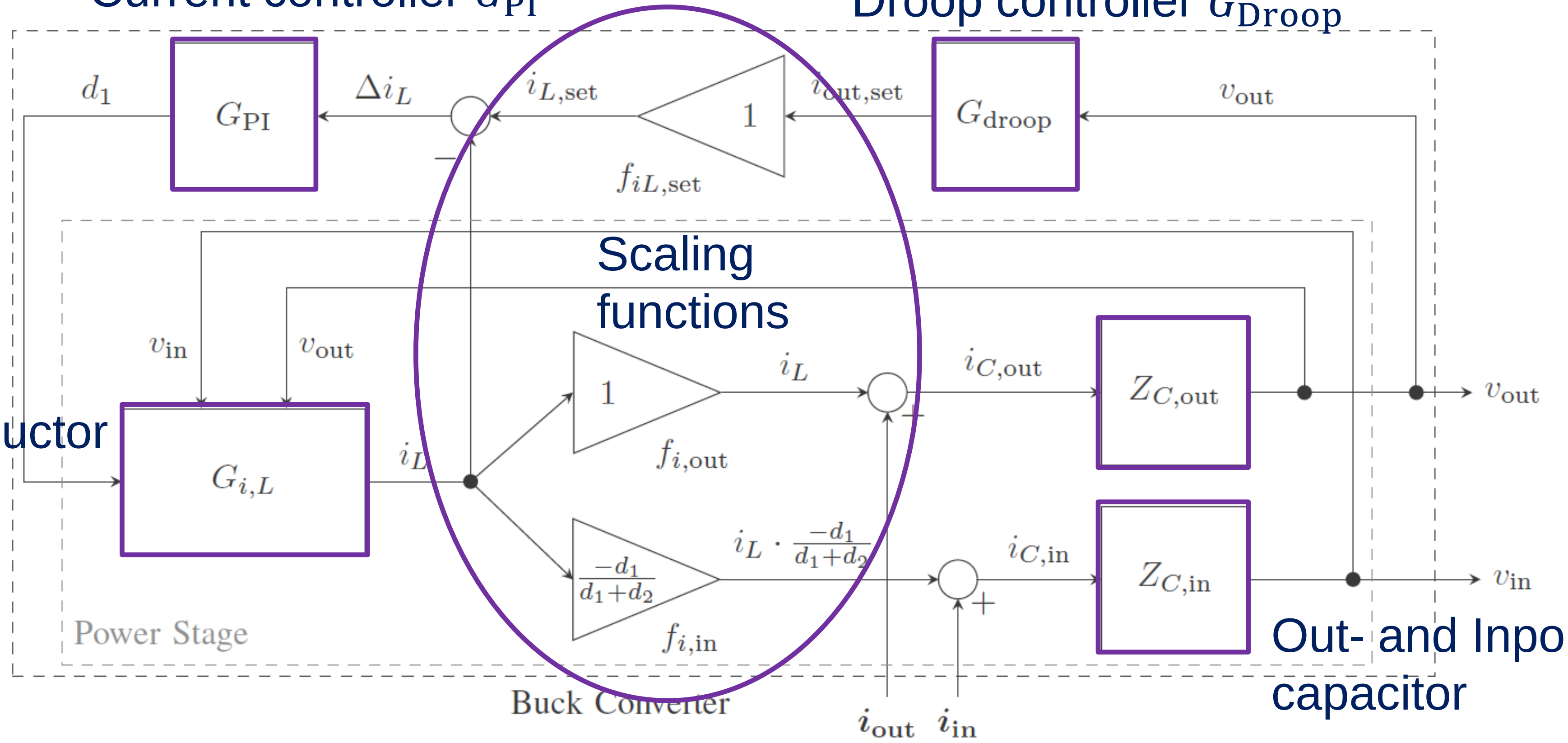
BUCK CONVERTER MODEL – LEVEL 3

Block diagram for converter model:

Modular Approach:

Converter components are grouped into functionally independent subsystems

➡ Individual sub-systems can be changed easily



Current controller G_{PI}

Droop controller G_{Droop}

Scaling functions

Averaged Switched-Inductor Stage $G_{i,L}$

Out- and Inport capacitor

Block Diagramm of Level 3 Buck converter model

BUCK CONVERTER MODEL – LEVEL 3

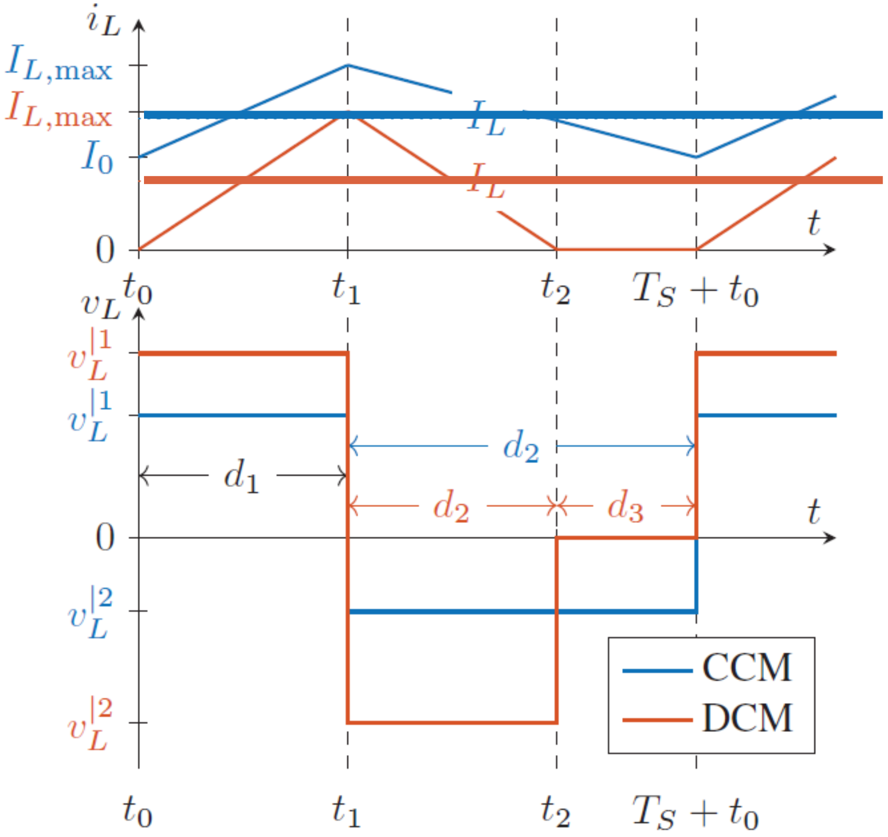
Averaged switch-mode converter modeling:

- Switched-inductor current $i_L(t)$ is averaged for one switching period T_S:

$$I_L = \frac{1}{T_S}\int i_L(t)\mathrm{d}t$$

- Switch modulation is represented by the duty ratios:

$$d_1 = \frac{t_{\mathrm{on,T1}}}{T_S} \text{ and } d_2 = \frac{t_{\mathrm{on,T2}}}{T_S}$$



Time dependent and averaged currents and voltages

BUCK CONVERTER MODEL – LEVEL 3

Equivalent circuit of power stage model:

Inport voltage:

Determined via inport and inductor current:

$$v_{\mathrm{C,in}} = \int \frac{i_{\mathrm{C,in}}}{\mathrm{C_{in}}}\,\mathrm{d}t$$

$$i_{\mathrm{C,in}} = i_{\mathrm{in}} - i_L \cdot \frac{d_1}{d_1 + d_2}$$

Switched-inductor current:

Determined via port voltages and d_1 and d_2:

$$i_L = \int \frac{v_L}{L}\,\mathrm{d}t$$

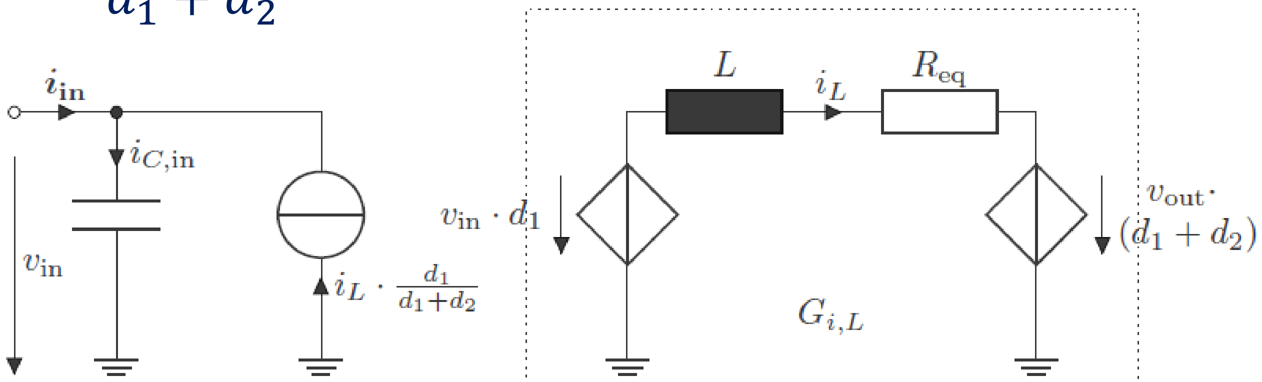
$$v_L = v_{\mathrm{in}} \cdot d_1 - v_{\mathrm{out}} \cdot (d_1 + d_2)$$

Outport voltage:

Determined via inductor and outport current:

$$v_{\mathrm{C,out}} = \int \frac{i_{\mathrm{C,out}}}{C_{\mathrm{out}}}\,\mathrm{d}t$$

$$i_{\mathrm{C,out}} = i_{\mathrm{out}} - i_L$$



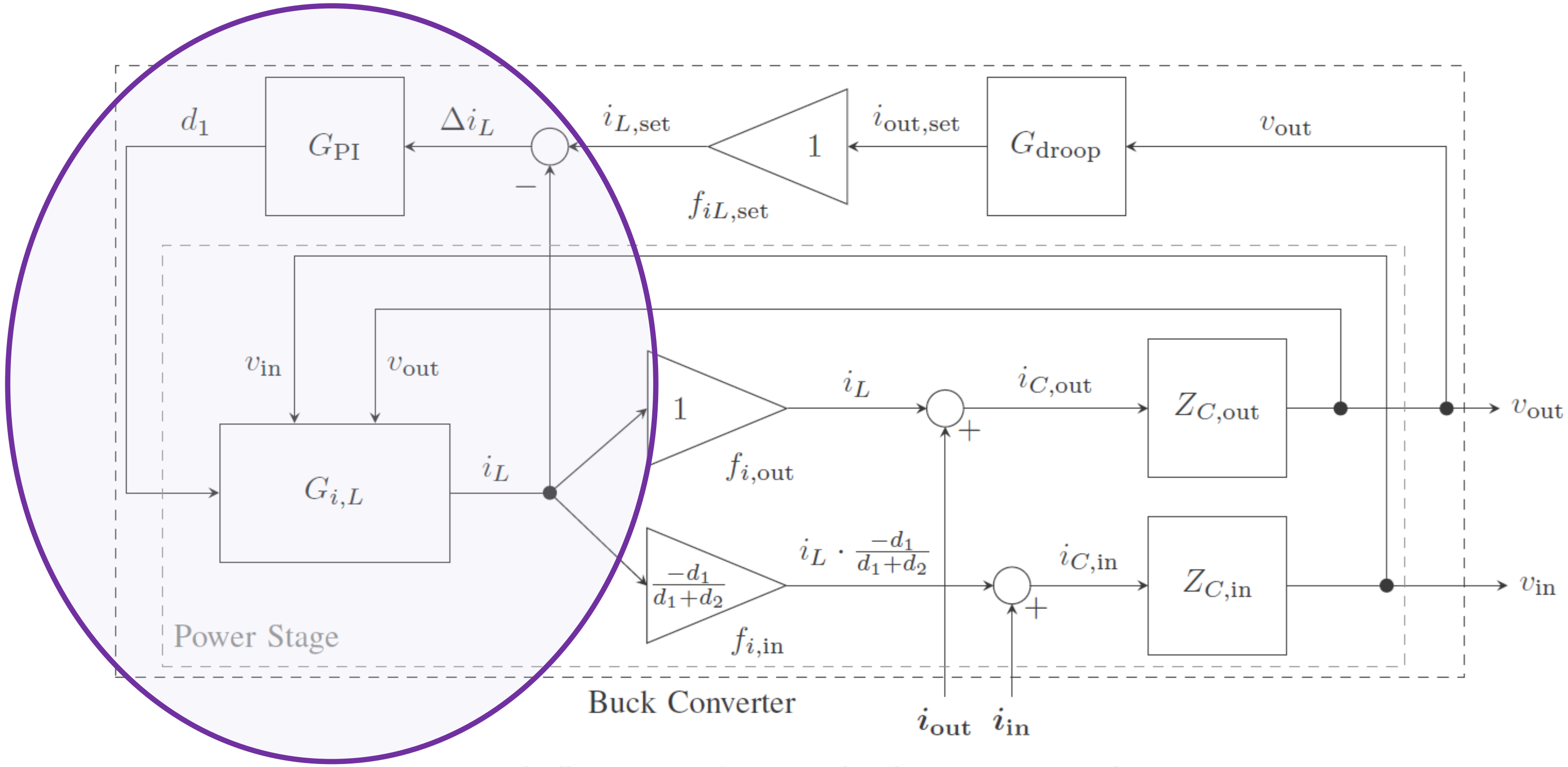
Equivalent Circuit of the Level 3 power stage

BUCK CONVERTER MODEL – LEVEL 2

Block diagram of converter model:

- Simplified current control dynamics
- Dynamics of closed inductor current control loop :

$$\frac{i_L}{i_{\mathrm{L,set}}} = \frac{i_{\mathrm{conv}}}{i_{\mathrm{out,set}}} = G_{\mathrm{conv}}$$



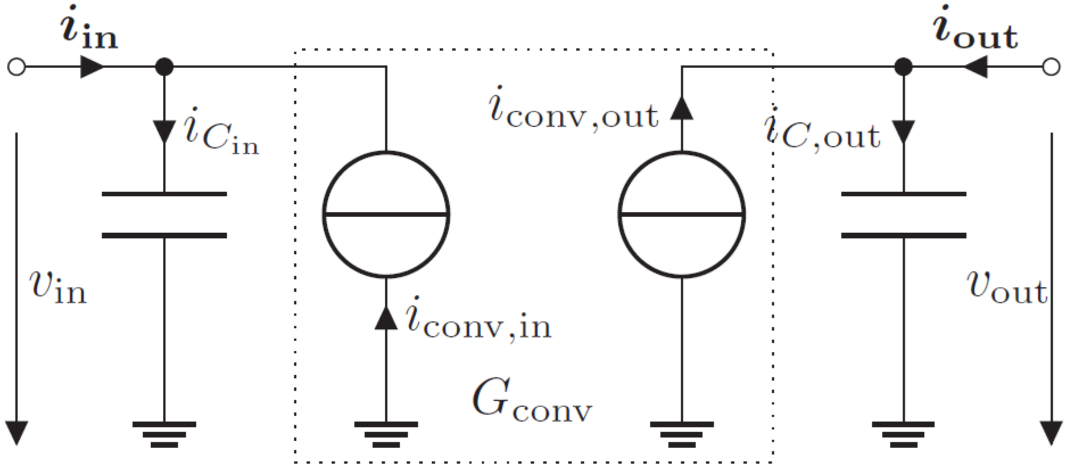
Block diagramm of Level 3 buck converter model

BUCK CONVERTER MODEL – LEVEL 2

Equivalent circuit of converter power stage:

- Switching-stage currents are determined via droop-control set current and simplified current control loop dynamics:

$$i_{\text{conv,in}} = \mathrm{M} \cdot i_{\text{Droop,set}} \cdot G_{\text{conv}}$$
$$i_{\text{conv,out}} = i_{\text{Droop,set}} \cdot G_{\text{conv}}$$



Equivalent circuit of the Level 2 power stage

➡ No differentiation between DCM and CCM

- Droop-control as well as in- and outport capacitor dynamics remain unchanged

BUCK CONVERTER MODEL – LEVEL 1

Equivalent circuit of converter power stage:

- Current control and switching dynamics reduced to transmission ratio

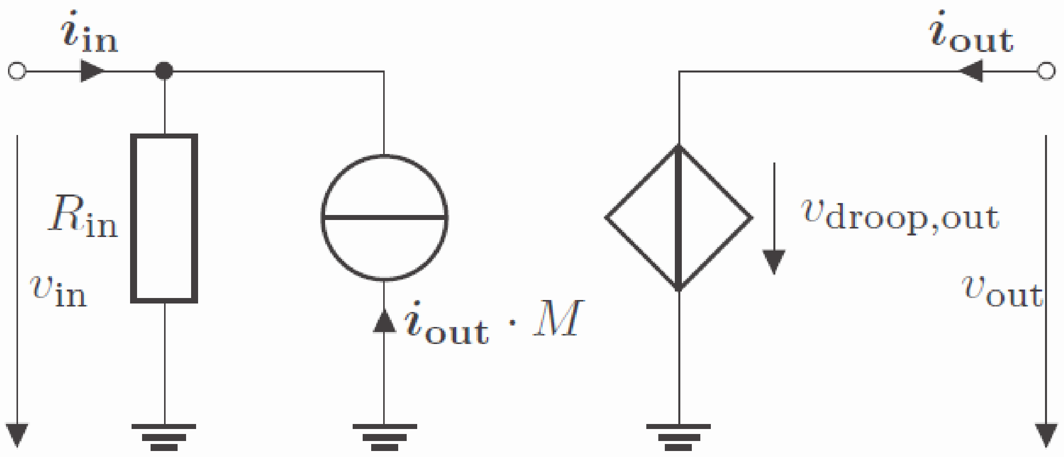
$$M = \frac{v_{\mathrm{out}}}{v_{\mathrm{in}}}$$

- Output voltage is determined by droop-control and output current

$$v_{\mathrm{out}} = i_{\mathrm{out}} \cdot G_{\mathrm{Droop}}$$

- Input voltage is determined via R_{in}:

$$v_{\mathrm{in}} = R_{\mathrm{in}} \cdot (i_{\mathrm{in}} - i_{\mathrm{out}} \cdot M)$$

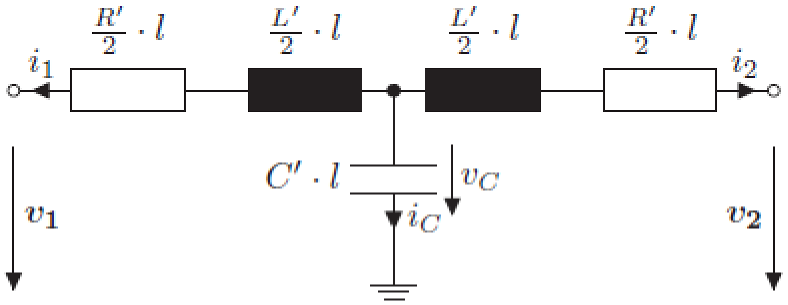


Equivalent circuit of the Level 1 power stage

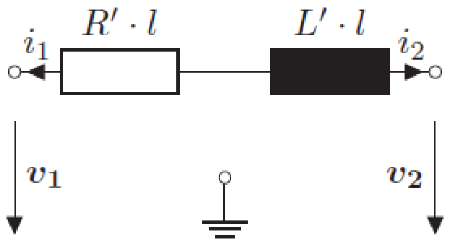
⇒ Limited interaction between out- and inport

LINE MODELING

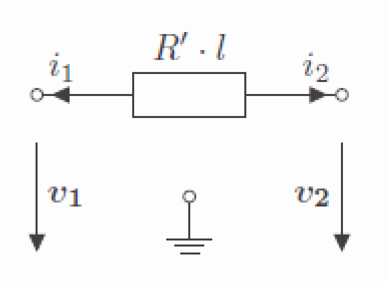
Equivalent circuits of line models:



Equivalent circuit of the Level 3 line model



Equivalent circuit of the Level 2 line model



Equivalent circuit of the Level 1 line model

Level 3 line models:

T-style lumped element model:

$$i_2 = \frac{v_C - v_L - v_2}{\frac{R'}{2} \cdot l}$$

$$i_1 = \frac{v_1 - v_L - v_C}{\frac{R'}{2} \cdot l}$$

Level 2 line models:

Capacitances are omitted:

$$i_2 = \frac{v_1 - v_2 - v_L}{R' \cdot l}$$

$$i_1 = -i_2$$

Level 1 line models:

Only resistive behavior:

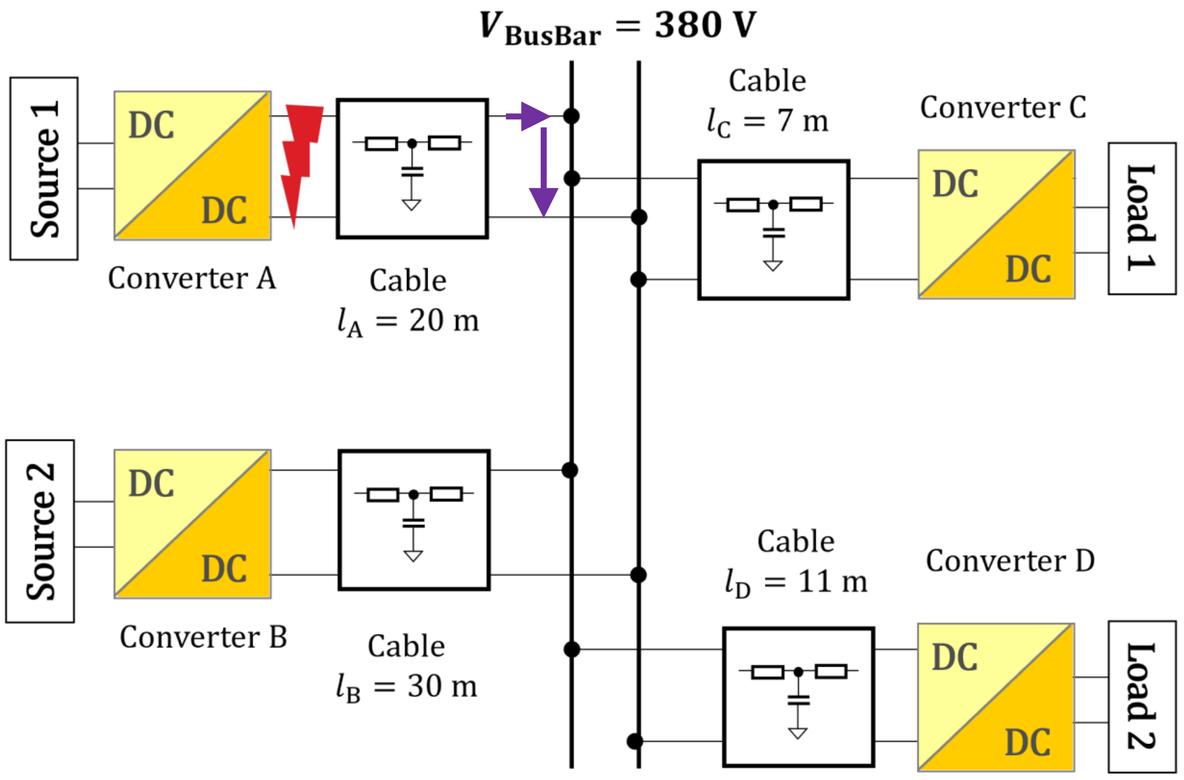
$$i_2 = \frac{v_1 - v_2}{R' \cdot l}$$

$$i_1 = -i_2$$

SIMULATION VS. MEASUREMENTS

Verification of simulated system behavior

- Four converters
  - Two droop-controlled source converters (Converters A and B)
  - Two constant power load converters (Converters C and D)
- Short circuit at outport terminal of Converter A with $R_{sc} = 10\ \mathrm{m\Omega}$
- Current i_{bus} and voltage v_{bus} at bus bar connection of Converter A



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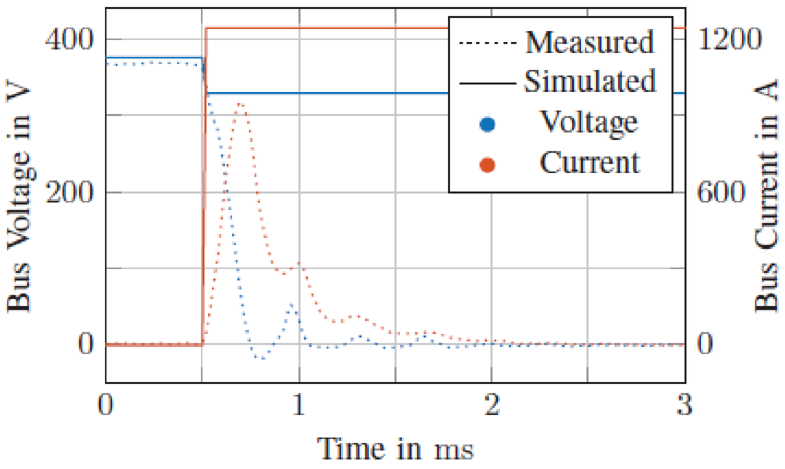
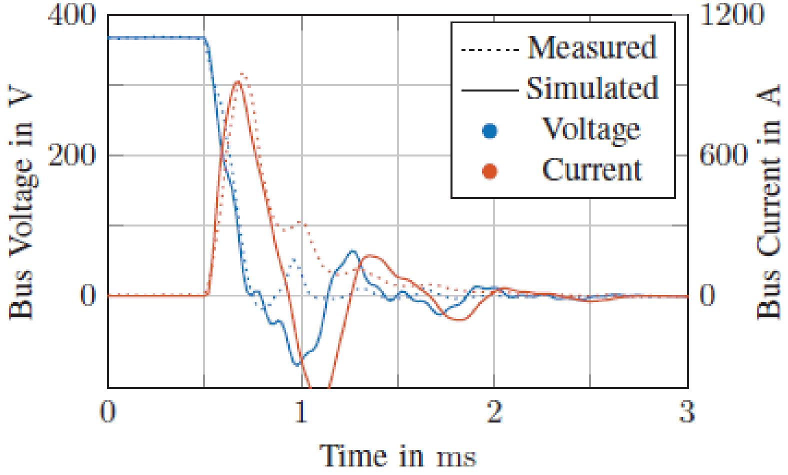
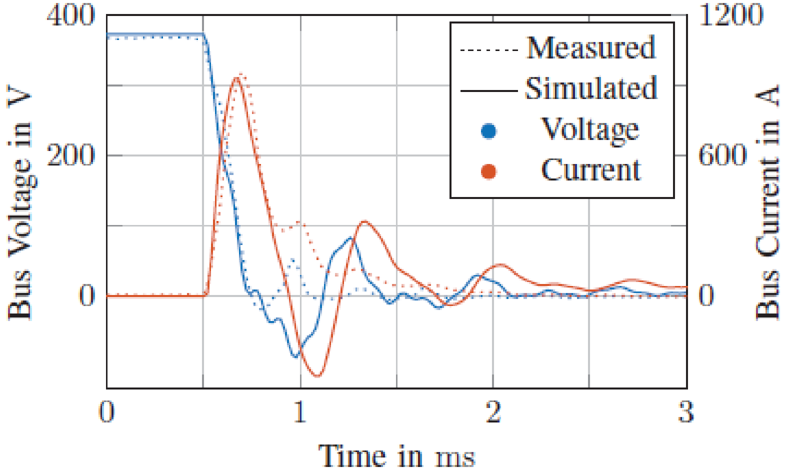
SIMULATION VS. MEASUREMENTS

Scenarios for different simulations of transient behavior







Setup I:
Level 1 Converter Model and
Level 1 Line Model

Intended Use Case:
Power Flow Analysis

Setup II:
Level 2 Converter Model and
Level 3 Line Model

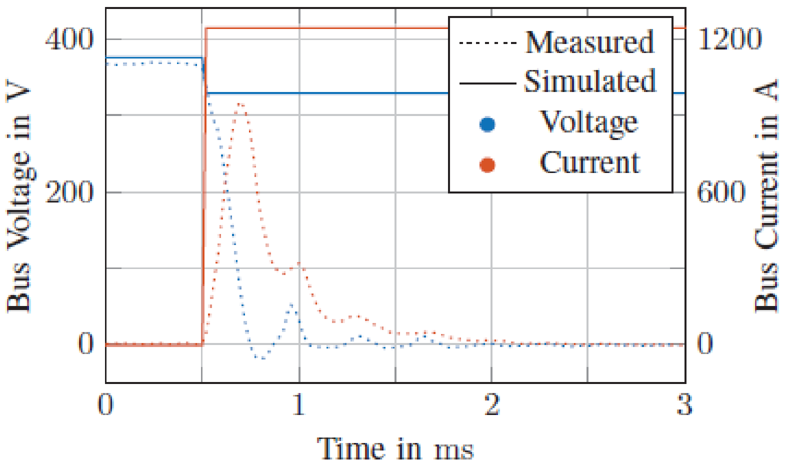
Intended Use Case:
Fault Behavior Analysis

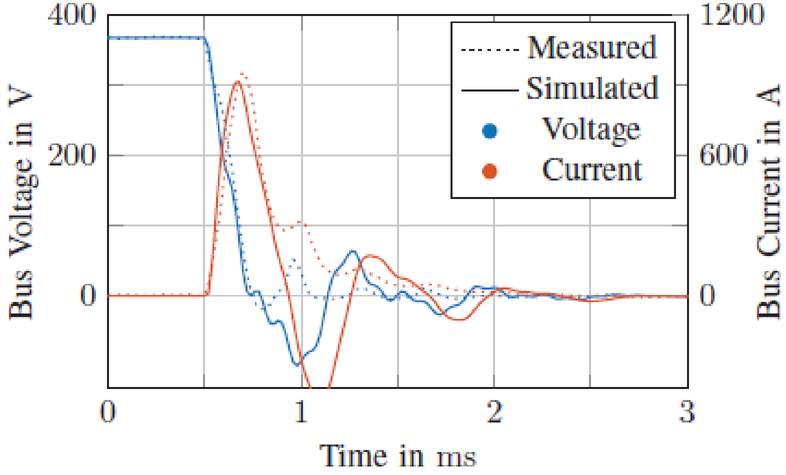
Setup III:
Level 3 Converter Model and
Level 2 Line Model

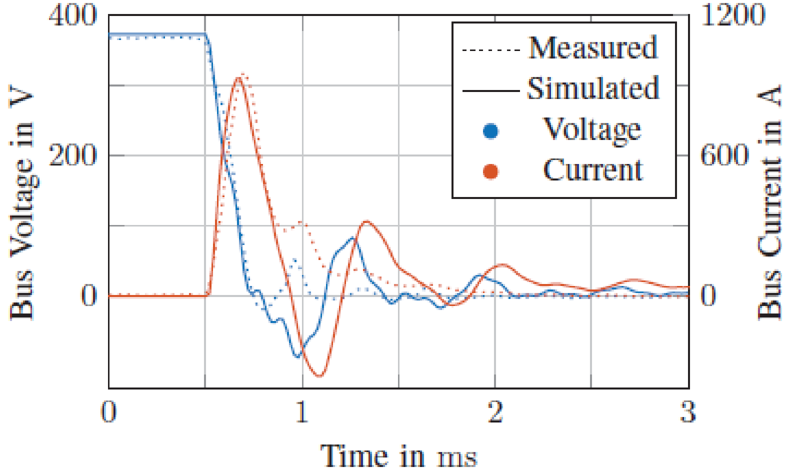
Intended Use Case:
System Stability Analysis

SIMULATION VS. MEASUREMENTS

Result comparison for measured $151\ \mathrm{A^2s}$ short circuit







Setup I:

Outport voltage and current have no dynamic behavior

Setup II:

Outport signals closely matches the measured signals

- $I^2t = 144\ \mathrm{A^2s}$
- Oscillations subside within the same time

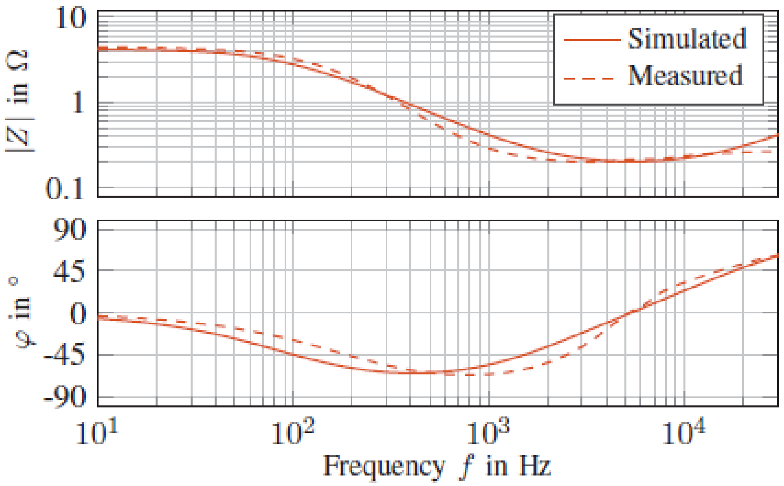
Setup III:

Outport signals closely matches the measured signals

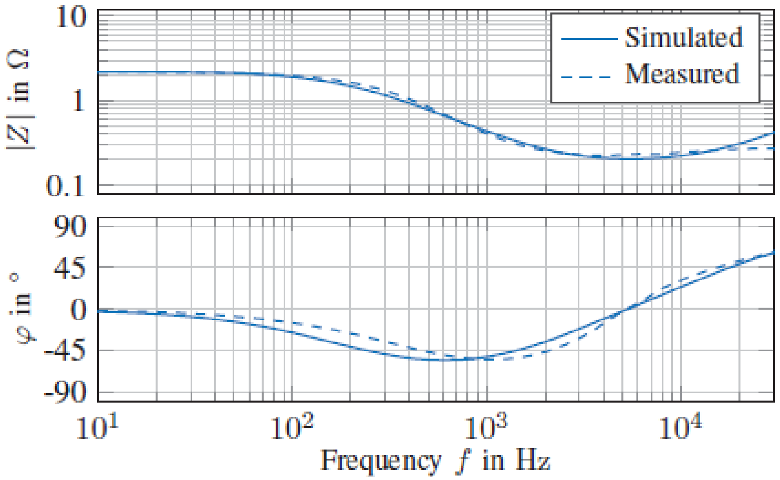
- $I^2t = 150\ \mathrm{A^2s}$
- Oscillations are much less damped

SIMULATION VS. MEASUREMENTS

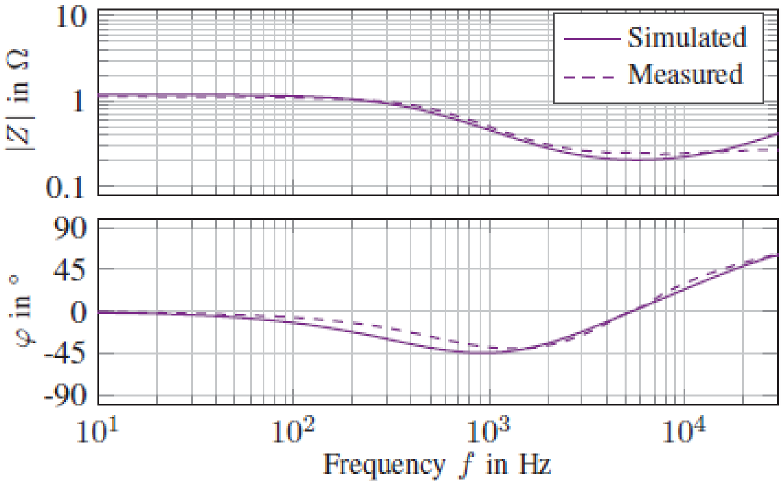
Output Impedances of Setup III:



Droop resistance $R_{\text{Droop}} = 4\ \Omega$



Droop resistance $R_{\text{Droop}} = 2\ \Omega$



Droop resistance $R_{\text{Droop}} = 1\ \Omega$

- Generally match the measured characteristics well
- Discrepancies around the drop-off frequency of the droop-control
- Best concordance for smallest droop resistance

CONCLUSIONS AND FURTHER WORKS

Initital verification of DC models in DC grid

- Reasons for discrepancies must be investigated and models optimized
- Computational Efficiency: Computation vs. simulation times evaluated
- Setup I behavior suitable for *Power Flow Analysis*
- Transient behavior of Setup II suitable for *Fault Behavior Analysis*
  - Current and voltage overshoot is too large
  - Dynamic behavior closest to measured behavior
- Impedance characteristics for Setup III suitabile for *System Stability Analysis*
  - Models overall match the measured impedance characteristics with small differences of φ
  - Slight discrepancies can be mitigated by adjusting analysis margins

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DC|hyPATwin
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